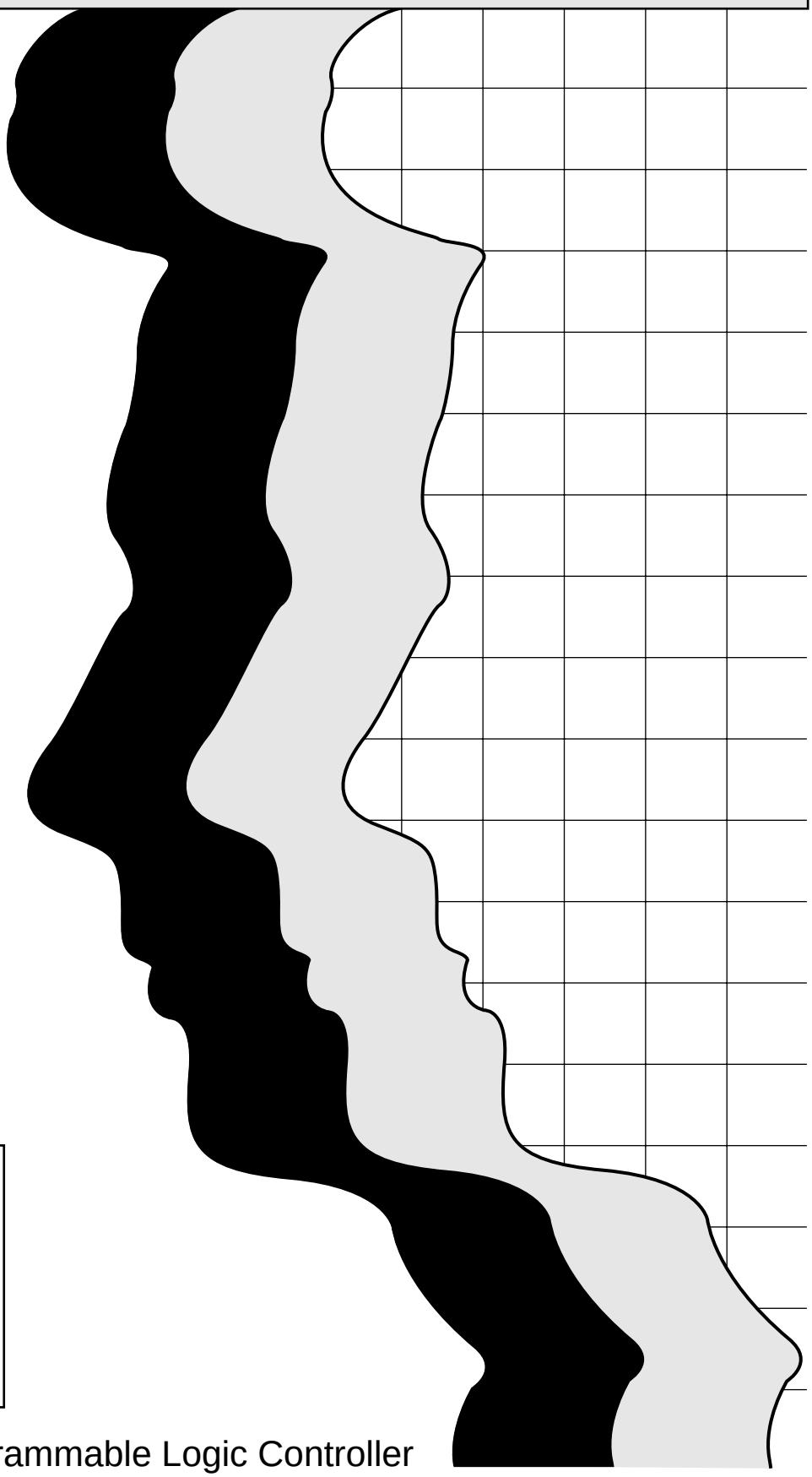
MITSUBISHI

D/A Converter Module Type A1S62DA

User's Manual



MELSEC

Mitsubishi Programmable Logic Controller

● SAFETY PRECAUTIONS ●

(Always read these instructions before using this equipment.)

Before using this product, please read this manual and the relevant manuals introduced in this manual carefully and pay full attention to safety to handle the product correctly.
The instructions given in this manual are concerned with this product. Refer to the User's Manual of the CPU module in use for details on the safety instructions for the programmable logic controller system.
In this manual, the safety instructions are ranked as "DANGER" and "CAUTION".

⚠ DANGER	Indicates that incorredt handling may cause hazardous conditions, resulting in death or severe injury.
⚠ CAUTION	Indicates that incorredt handling may cause hazardous conditions, resulting in medium or slight personal injury or physical damage.

Note that the ⚠ **CAUTION** level may lead to a serious consequence according to the circumstances. Always follow the instructions of both levels because they are important to personal safety.

Please save this manual to make it accessible when required and always forward it to the end user.

[DESIGN PRECAUTIONS]

⚠ DANGER

- Install a safety circuit external to the PLC that keeps the entire system safe even when there are problems with the external power supply or the PLC module.
  Otherwise, trouble could result from erroneous output or erroneous operation.
  (1) The analog output state will differ according to the setting state of the various functions for controlling the analog output.
  Take special care when making the settings.
  Refer to Section 3.3.2 for details on the analog output state.
  (2) If there is a fault in the output element or the internal circuit, correct outputs may not be possible or erroneous outputs may be made.
  Provide a circuit to externally monitor output signals that could lead to major faults.

⚠ CAUTION

- Do not bunch the control wires or conmmunication cables with the main circuit or power wires, or install them close to each other.
  They should be installed 100mm (3.94inch) or more from each other.
  Not doing so could result in noise that would cause erroneous operation.

[INSTALLATION PRECAUTIONS]

⚠ CAUTION

- Use the PLC in an environment that meets the general specifications given in the User's Manual of the CPU module in use.
  Using this PLC in an environment outside the range of the general specifications could result in electric shock, fire, erroneous operation, and damage to or deterioration of the product.
- Install so that the pegs on the bottom of the module fit securely into the base unit peg holes and use the specified torque to tighten the module's fixing screws. Not installing the module correctry could result in erroneous operation, damage, or pieces of the product falling.
  Tightening the screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunctions.
- Do not directly touch the module's conductive parts or electronic components.
  Touching the conductive parts could cause an operation failure or give damage to the module.
- Tighten the terminal screws with the specified torque.
  If the terminal screws are loose, it could result in short circuits, five or erroneous operation.
  Overtightening can cause a drop, short circuits or malfunction due to damage to the screw or module.

[WIRING PRECAUTIONS]

⚠ CAUTION

- When wiring in the PLC, be sure that it is done correctly by checking the product's rated voltage and the terminal layout.
  Connecting a power supply that is different from the rating or incorrectly wiring the product could result in fire or damage.
- Tighten the terminal screws with the specified torque.
  If the terminal screws are loose, it could result in short circuits, fire, or erroneous operation.
  Overtightening can cause a drop, short circuits or malfunction due to damage to the screw or module.
- Be sure there are no foreign substances such as sawdust or wiring debris inside the module.
  Such debris could cause fires, damage, or erroneous operation.

[STARTUP AND MAINTENANCE PRECAUTIONS]

⚠ CAUTION

- Do not touching the terminals with power on.
  Failure to observe this could lead to erroneous operation.
- **Be sure to shut off all phases of the external power supply used by the system before cleaning or retightening the terminal screws.**
  Not doing so can cause a module failure or malfunction.
  If the terminal screws are loose, it could result in short circuits, five or erroneous operation.
  Overtightening can cause a drop, short circuits or malfunction due to damage to the screw or module.
- Do not disassemble or modify the module.
  Doing so could cause trouble, erroneous operation, injury, or fire.

[STARTUP AND MAINTENANCE PRECAUTIONS]

⚠ CAUTION

- **Be sure to shut off all phases of the external power supply used by the system before mounting or dismounting the module.**
  If you do not switch off the external power supply, it will cause failure or malfunction of the module.
- Do not install/remove the terminal block more than 50 times after the first use of the product. (IEC 61131-2 compliant)
- Before handling the module, always touch grounded metal, etc. to discharge static electricity from the human body.
  Failure to do so can cause the module to fail or malfunction.

[DISPOSAL PRECAUTIONS]

⚠ CAUTION

- When disposing of the product, handle it as industrial waste.

REVISIONS

*The manual number is given on the bottom left of the back cover.

Print Date	*Manual Number	Revision
Sep., 1991	IB (NA) 66335-A	First edition
Apr., 2001	IB (NA) 66335-B	Addition SAFETY PRECAUTIONS, WARRANTY Correction Section 1.1, Chapter 2, Section 3.1, 3.2, 3.3, 3.3.2, 3.6.1, 3.7.1, 3.7.3, 4.2, 4.5, 4.5.2, 4.6.2, 5.1, 5.2, 5.3, 6.8, 6.9 Delection 6.7
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Japanese Manual Version SH-3526-I

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

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Conformation to the EMC Directive and Low Voltage Instruction

For details on making Mitsubishi PLC conform to the EMC directive and low voltage instruction when installing it in your product, please see Chapter 3, "EMC Directive and Low Voltage Instruction" of the User's Manual (Hardware) of the PLC CPU to use.

The CE logo is printed on the rating plate on the main body of the PLC that conforms to the EMC directive and low voltage instruction.

By making this product conform to the EMC directive and low voltage instruction, it is not necessary to make those steps individually.

1. INTRODUCTION

This manual describes specifications, handling, programming and other information on the A1S62DA digital-to-analog converter module (referred to as "A1S62DA") for use with a MELSEC-A series A1SCPU module (hereafter called the CPU).

A1S62DA is used to convert incoming digital values (16-bit signed binary data) which are set with the PLC CPU to analog valtage.

1.1 Features

A1S62DA has the following features.

(1) Allows digital-to-analog conversion for 2 channels.

The A1S62DA can output the analog values to 2 external devices.
Or, voltage output and amperage output are selected for each channel.

(2) Allows setting of the resolution of digital values at three stages (all the channels in a batch).

Resolution of the digital values may be set by selecting from 1/4000, 1/8000 and 1/120000 by resolution setting.

(3) Allows the analog output to be enabled/disabled on a channel basis.

The value of the analog output may be enabled or disabled for each channel using the sequence program.

The channel that is disabled for the analog output provides an analog output value of 0 V or 0 mA.

(4) Allows the setting of the analog output to be held or cleared (all channels in batch) at STOP of the CPU.

The holding of the analog output, when the CPU is at STOP may be set with the HOLD/CLEAR terminal.

(5) Allows an offset/gain adjustment to be made without using the offset/gain adjusting knobs.

The offset and gain values may be specified by using the UP/DOWN switch for each channel.

2. SYSTEM CONFIGURATIONS

(1) Applicable CPUs

- A1SJCPU(S3)
- A1SJHCPU(S8)
- A1SCPU(S1)
- A1SCPUC24-R2
- A1SHCPU
- A2SCPU(S1)
- A2SHCPU(S1)
- A2USCPU(S1/S30)
- A2USHCPU-S1
- Q2ASCPU(S1)
- Q2ASHCPU(S1)
- A52GCPU
- Q02(H)CPU-A
- Q06HCPU-A

(2) Number of mounted modules

There is no limit to the number of modules that can be used as long as the total is within the input point range for the applicable CPU.

(3) Mounting slot

The module can be mounted into a random slot on the base unit, except in the following cases.
If the module is mounted into an extesion base unit (A1S52B, A1S55B,A1S58B) having no power supply unit, the power capacity may be insufficicient. When mounting the A1S62DA onto an extension base unit with no power supply unit, consider the following matters.

1) Current capacity of power supply unit on main base unit.
2) Voltage drop at main base unit.
3) Voltage drop at extension base unit.
4) Voltage drop at extension cable.

Select the power supply unit, main base unit, extension base unit and extension cables taking the above matters into consideration.

(4) Precautions for using 2 channels in A1S62DA.

Photocoupler insulation is used for A1S62DA between an output terminal and the PLC power. However, the earth terminal of the analog output is connected inside.

Therefore, the"—V" signals and "—I" signals of eacha channel become the same levels.

(5) Data link system

In the data link system, the CPU can be mounted onto the master station, local station or remote I/O station. Refer to the MELSACNET and MELSACNET/B Data Link System Reference Manual for examples of the remote I/O station programs.

REMARKS

Refer to the CPU module user's manuals for details on the range of number of occupied I/O points and the method of calculatiing the voltage drop.

3. SPECIFICATIONS

This chapter describes the general specifications, performance specifications, and I/O conversion characteristics of the A1S62DA.

3.1 General Specifications

Table 3.1 shows the general specifications of the A1S62DA.

Table 3.1 General Specifications

Item	Specifications				
Operating ambient temperature	0 to 55°C				
Storage ambient temperature	–20 to 75°C				
Operating ambient humidity	10 to 90%RH, non-condensing				
Storage ambient humidity	10 to 90%RH, non-condensing				
Vibration resistance	Conforms to JIS B 3502, IEC61132-2	Frequency	Acceleration	Amplitude	Sweep Count
		10 to 55Hz	—	0.075mm	10 times *(1 octave/ minute)
		55 to 150Hz	9.8m/S²	—	
Shock resistance	Conforming to JIS B 3502, IEC61132-2 (147m/S², 3time each in 3directions)				
Noise durability	By noise simulator of 1500 Vpp noise voltage, 1 μs noise width and 25 to 60Hz noise frequency.				
Dielectric withstand voltage	1500 VAC for 1 minute across AC external terminals and ground 500 VAC for 1 minute across DC external terminals and ground				
Insulation resistance	500MΩ or larger by 500 VDC insulation resistance tester across AC external terminals and ground				
Grounding	Class 3 grounding; grounding is not required when it is impossible.				
Operating ambience	Free of corrosive gases. Dust should be minimal.				
Cooling method	Self-cooling				

REMARK

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10Hz to 20Hz, from 20Hz to 40Hz, from 40Hz to 20Hz, and 20Hz to 10Hz are referred to as one octave.

3.2 Performance Specifications

Table 3.2 shows the performance specifications of the A1S62DA.

Table 3.2 Performance Specifications

Item		Specifications							
		Voltage Output				Current Output			
Digital input	1/4000 1/8000 1/12000	−4000 to 4000 −8000 to 8000 −12000 to 12000				0 to 4000 0 to 8000 0 to 12000			
Analog output		−10 to 0 to 10 VDC (External load resistance: 2 KΩ to 1 MΩ)				0 to 20 mADC (External load resistance: 0 to 600 Ω)			
I/O characteristics	Resolution	1/4000	1/8000	1/12000	Analog output value *1	1/4000	1/8000	1/12000	Analog output value *2
	Digital input value	4000 2000 0 −2000 −4000	8000 4000 0 −4000 −8000	12000 6000 0 −6000 −12000	10 V 5 V 0 V −5 V −10 V	4000 2000 0	8000 4000 0	12000 6000 0	20 mA 12 mA 4 mA
Maximum resolution of analog value	1/4000 1/8000 1/12000	2.5 mV 1.25 mV 0.83 mV			(10 V) (10 V) (10 V)	5 μA 2.5 μA 1.7 μA			(20 mA) (20 mA) (20 mA)
Overall accuracy (accuracy to the maximum value)		±1.0% (±100mV)				±1.0% (±200 μA)			
Maximum conversion time		Maximum 25 ms/2 channels (same for 1 shannel)							
Absolute maximum output		Voltage: ±12 V Current: 28 mA							
Output short circuit protection		Provided							
Analog output points		2 channels/module							
Insulation method		Photocoupler insulation between output terminals and PLC power No insulation between channels							
Number of I/O points		Special 32 points							
Connection terminal		20 point terminal block							
Offset/gain adjustment		By the test switch (without using offset/gain adjusting knobs)							
Applicable wire size		0.75 to 1.5 mm^2							
Applicable solderless terminal		1.25-3, 1.25-YS3A, V1.25-3, V1.25-YS3A							
Internal current consumption (5 VDC)		0.8 A							
Weight		0.32kg							

*1....When the offset value is set to 0 V and the gain value is set to 10 V.

*2....When the offset value is set to 4 mA and the gain value is set to 20 mA.

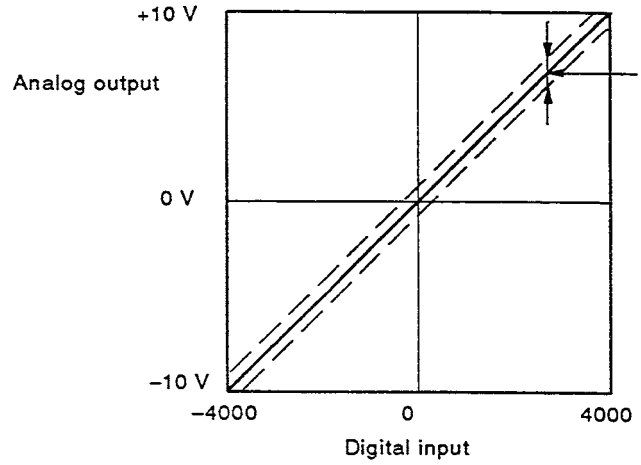
*3, *4....See the following page.

A power supply module is not required.

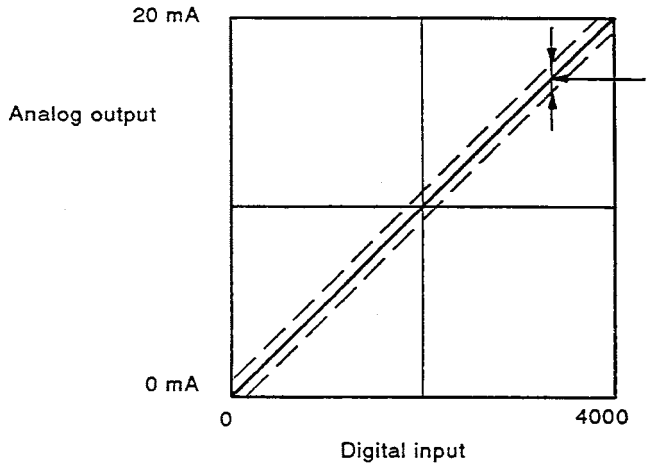
*3 Overall accuracy

The overall accuracy is the accuracy to the maximum value of analog output.

(a) Overall accuracy of the voltage output is the accuracy when the output voltage setting is 10 volts.



(b) Overall accuracy of the current output is the accuracy when the output voltage setting is 20 mA.



*4 The maximum conversion speed is the time from inputting the digital value to outputting the analog value.

3.3 I/O Conversion Characteristics

The following explains the I/O conversion characteristics of A1S62DA.

(1) I/O conversion characteristics

I/O characteristics are provided to convert a digital value specified from the CPU into an analog value and are indicated by an inclination connected between an offset value and a gain value.

(2) Offset/gain values

(a) The offset and gain values are defined as follows.

1) Offset value

Voltage output from the A1S62DA when the digital value specified from the PLC CPU is "0".

2) Gain value

Voltage output from the A1S62DA when digital value specified from the PLC CPU is "4000" (when digital value resolution setting is 1/4000).

(b) Offset/gain values are set before delivery as shown below.

	Voltage Output
Offset value:	0 V
Gain value:	10 V

(c) Offset/gain value can be changed for each channel in the test mode.

3.3.1 Voltage output

(1) I/O conversion characteristic example

The figure below shows an example of I/O conversion characteristics.

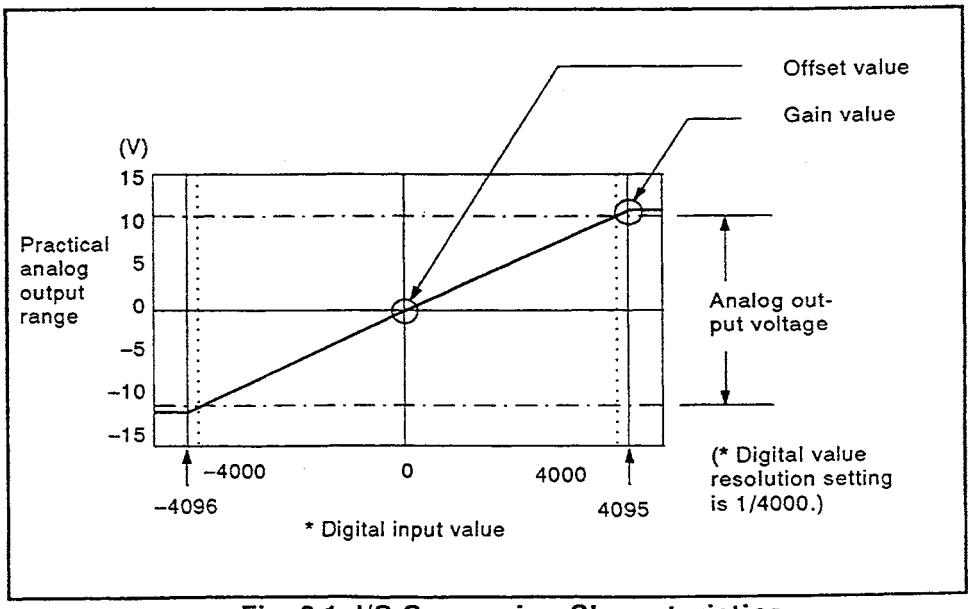


Fig. 3.1 I/O Conversion Characteristics

(2) Relation between the offset/gain values and the analog output

Resolution of the A1S62DA can be changed as appropriate by offset/gain setting.

Resolution of the analog value and analog output that are caused by digital input when offset/gain setting is changed are obtained as shown below.

$$\text{(Resolution of analog value)} = \frac{\text{(Gain value)} - \text{(Offset value)}}{\text{(Resolution of digital value)}}$$

$$\text{(Analog output)} = \frac{\text{(Gain value)} - \text{(Offset value)}}{\text{(Resolution of digital value)}} \times \text{(Digital input)} + \text{(Offset value)}$$

$$= \text{(Resolution of analog value)} \times \text{(Digital input)} + \text{(Offset value)}$$

As shown in Table 3.2 Performance Specifications, the maximum of the analog value resolution of the A1S62DA varies with the resolution setting.

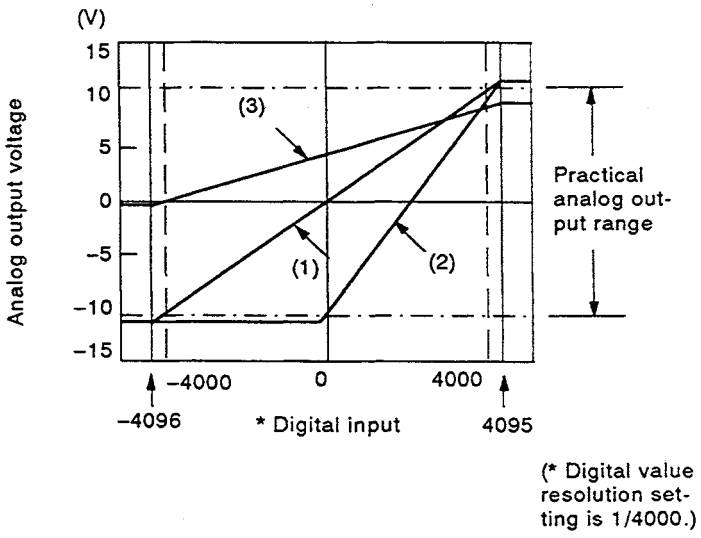
The variation of the analog output value for a change of 1 in the digital input value may not be calculated as shown above.

(3) I/O conversion characteristics when the offset/gain setting is changed

The figures below show the I/O conversion characteristics when offset/gain setting is changed.

The right figure shows the I/O conversion characteristics when offset/gain setting is provided as follows.

No.	Offset Value	Gain Value
(1)	0 V	+10 V
(2)	−10 V	+10 V
(3)	+4 V	+8 V



Example:

(1) The analog output voltages are as follows at the digital input value settings of 2000 and 500 for the characteristic graphs (1) to (3).

No.	Digital Input	Analog Output
(1)	2000	+5.0 V
	500	+1.25 V
(2)	2000	0 V
	500	−5.0 V
(3)	2000	6.0 V
	500	1.5 V

Fig. 3.2 I/O Conversion Characteristics When Offset/Gain Setting is Changed

3.3.2 Current output

(1) I/O conversion characteristic example

The figure below shows an example of I/O conversion characteristics.

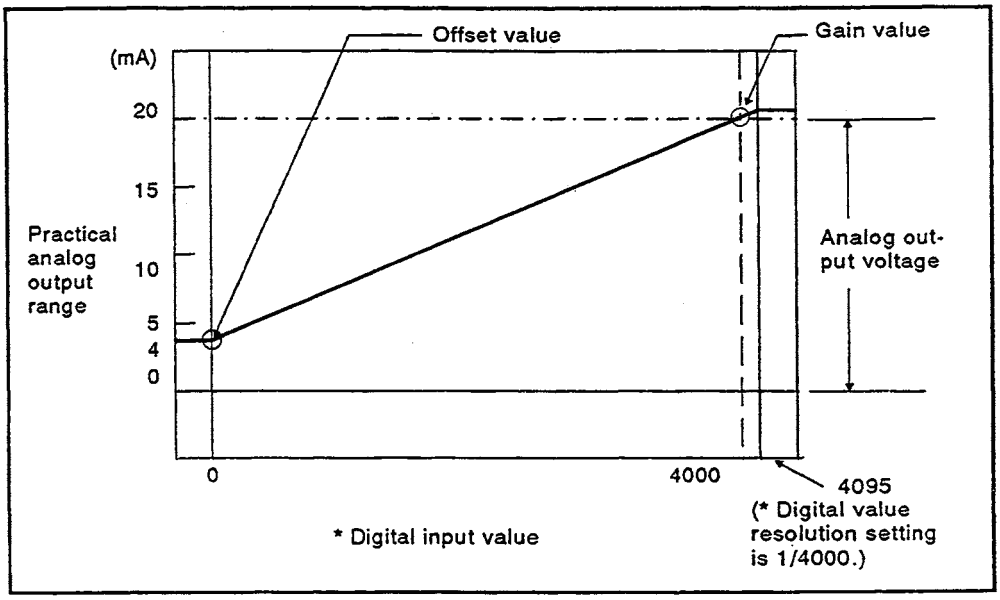


Fig. 3.3 I/O Conversion Characteristics

(2) Relation between the offset/gain values and the analog output

Resolution of the A1S62DA can be changed as appropriate by offset/gain setting.

However, an offset/gain value less than 0 mA cannot be set. If the value is set incorrectly, an error may not occur, but an analog output error may occur.

Resolution of the analog value and the analog output that are caused by the digital input when offset/gain setting is changed are obtained as shown below.

$$\text{(Resolution of analog value)} = \frac{\text{(Gain value)} - \text{(Offset value)}}{\text{(Resolution of digital value)}}$$

$$\text{(Analog output)} = \frac{\text{(Gain value)} - \text{(Offset value)}}{\text{(Resolution of digital value)}} \times \text{(Digital input)} + \text{(Offset value)}$$

$$= \text{(Resolution of analog value)} \times \text{(Digital input)} + \text{(Offset value)}$$

As shown in Table 3.2 Performance Specifications, the maximum of the analog value resolution of the A1S62DA varies with the resolution setting.

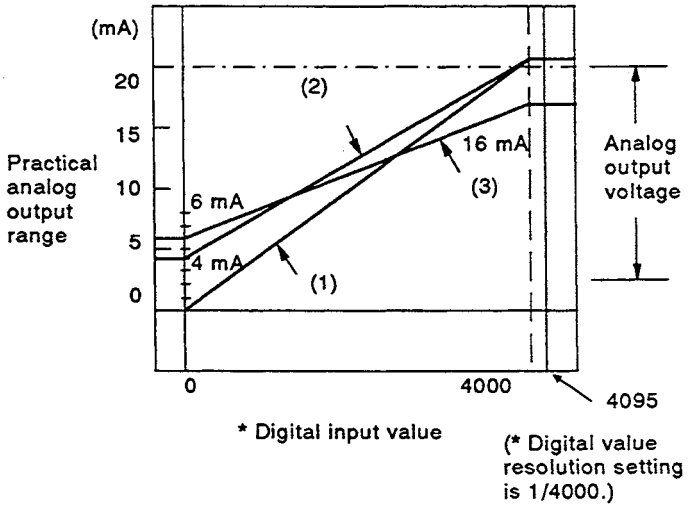
The variation of the analog output value for a change of 1 in the digital input value may not be calculated as shown above.

(3) I/O conversion characteristics when the offset/gain setting is changed

The figures below show the I/O conversion characteristics when the offset/gain setting is changed.

The right figure shows the I/O conversion characteristics when offset/gain setting is provided as follows.

No.	Offset Value	Gain Value
(1)	0 mA	20 mA
(2)	4 mA	20 mA
(3)	6 mA	16 mA



Example

(1) The analog output voltages are as follows at the digital input value settings of 2000 and 1000 for the characteristic graphs (1) to (3).

No.	Digital Input	Analog Output
(1)	2000	10 mA
	1000	5 mA
(2)	2000	12 mA
	1000	8 mA
(3)	2000	11 mA
	1000	8.5 mA

Fig. 3.4 I/O Conversion Characteristics When Offset/Gain Setting is Changed

3.4 Analog Output Control Functions

The following explains the function of each of the controls for the analog output of A1S62DA.

3.4.1 Analog output HOLD/CLEAR function at STOP of CPU

When the CPU is at STOP, or when the D-A conversion is stopped by the CPU module because of an error, holding of analog output may be selected for all channels in the batch with the HOLD/CLEAR terminal.

3.4.2 D-A conversion execute/non-execute setting function (D-A conversion output enable flag)

This function determines if each channel outputs a D-A conversion value or an offset value by setting a D-A conversion value output enable flag for each channel in the sequence program.

The D-A conversion time (conversion speed) is fixed regardless of setting a D-A conversion value disable flag.

ON : D-A conversion value

OFF: Offset value

3.4.3 Analog value external output enable/disable setting function (analog output enable/disable)

This function determines if an analog value output to external devices is enabled or disabled by writing 0/1 to address 0 for each channel in the sequence program.

Select one of the functions according to the state of the analog output to be set.

3.4.4 Function combination

When the CPU is at RUN or STOP, or when an error occurs in the CPU, analog values can be set as shown in Table 3.3 by combining any or all of the analog output control functions. Select the most appropriate combination.

Table 3.3 Analog Output State Setting Combinations

Setting Combination / Output Status	HOLD/CLEAR Setting	CLEAR				HOLD	
	D-A Conversion Output Enable Flag	Enable (ON)		Disable (OFF)		Enable (ON) / Disable (OFF)	
	Analog Output Enable/Disable Setting	Enable (0)	Disable (1)	Enable (0)	Disable (1)	Enable (0)	Disable (1)
Analog output at CPU STOP		Analog value after D-A conversion of digital value set with the PLC CPU is output/	0 V/0 mA	Offset value is output.	0 V/0 mA	Analog value after D-A conversion of digital value set with the PLC CPU is output/	0 V/0 mA
Analog output at CPU STOP		Offset value is output.	0 V/0 mA	Offset value is output.	0 V/0 mA	Analog value before STOP is held.	0 V/0 mA
Analog output at CPU error occurrence		0 V/0 mA	0 V/0 mA	0 V/0 mA	0 V/0 mA	0 V/0 mA	0 V/0 mA
Analog output at A1S62DA error occurrence		Analog value of the high or low limit is output.	0 V/0 mA	Offset value is output.	0 V/0 mA	Analog value of the high or low limit is output.	0 V/0 mA

3.5 Function Block Diagram

The following shows the function block diagram of A1S62DA.

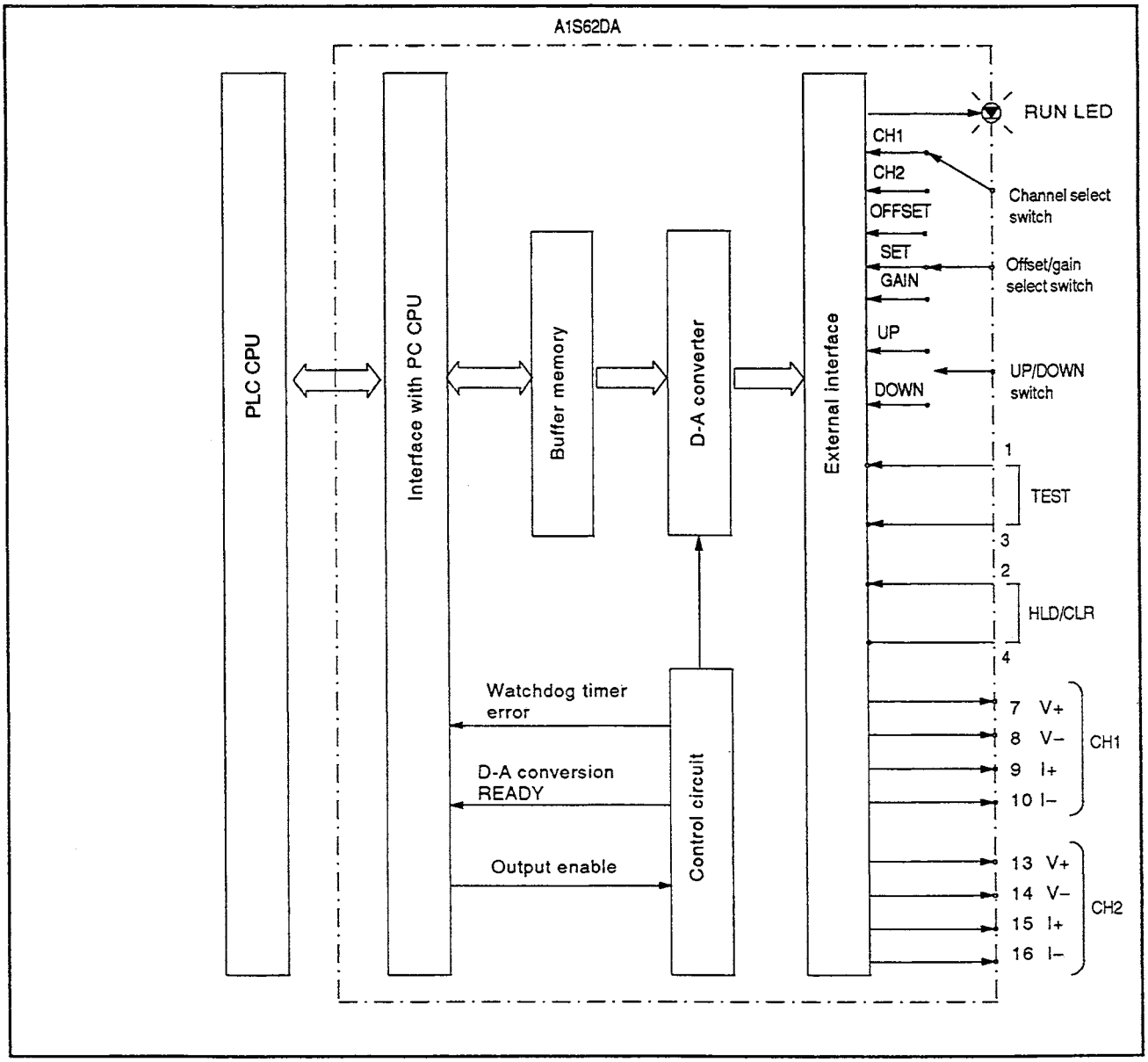


Fig. 3.5 A1S62DA Function Block Diagram

3.6 CPU I/O Signal

This section explains the allocation of I/O signals and the function of each signal.

3.6.1 Overview of I/O signals

The A1S62DA uses 32 signal points for input and output respectively.

Table 3.4 gives the allocation and description of I/O signals.

X devices refer to input signals from the A1S62DA to the CPU.

Y devices refer to output signals from the CPU to the A1S62DA.

The device numbers (input signals) shown in the table are used when the A1S62DA is loaded into slot 0 of the main base unit.

Table 3.4 I/O Signals

Signal Direction: A1S62DA → CPU		Signal Direction: CPU → A1S62DA	
Device No.	**Signal Description**	**Device No.**	**Signal Description**
X0	WDT error flag (A1S62DA detection)	Y0 through YF	Prohibited
X1	D-A conversion READY		
X2	Error flag		
X3 through X1F	Prohibited	Y10	CH1 D-A conversion output enable flag
		Y11	CH2 D-A conversion output enable flag
		Y12 through Y17	Prohibited
		Y18	Error reset
		Y19 through Y1F	Prohibited

IMPORTANT

Because devices Y0 through YF, Y12 through Y17, and Y19 through Y1F are used in the system, they cannot be used in the sequence program.

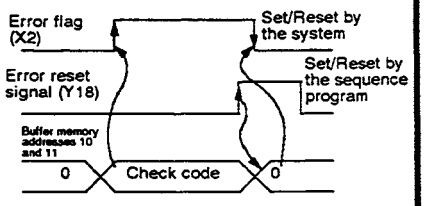
If any of these devices are used (turned ON/OFF) in the sequence program, the functions of the A1S62DA cannot be guaranteed.

If any of the devices Y0 through YF, has the same number as any of the devices X0 through XF, that device cannot be used as an internal relay.

3.6.2 I/O signal functions

The following table explains the function of each I/O signal of A1S62DA.

Table 3.5 I/O signal functions

Device No.	Signal	Description	Remark
X0	WDT (watch dog timer error flag)	• This flag is set when the self-diagnosis function of the A1S62DA detects a WDT error.	While the error flag is set, the D-A conversion of the A1S62DA does not RUN. If the error flag (X0) is set, hardware malfunction may occur.
X1	D/A conversion READY signal	• This signal is turned ON when the D/A conversion is ready after turning on or resetting the CPU in a mode other than the normal mode (test mode). • If the test terminals on the front of the module are connected to each other, this signal is turned OFF. • The D/A conversion READY signal (X1) can also be used as the buffer memory read/write interlock .	In this manual, "D/A conversion READY" means the time when the analog output values have been output to external equipment by executing the D/A conversion with each channel.
X2	Error flag	• This flag is set when an error other than the watch dog timer error occurs in the A1S62DA. • If the error reset signal is set or "0" is written to the setting value check code storage area for 2 channels, X2 is reset.	
Y10 Y11	D-A conversion output enable flag	• If any of the D-A conversion enable flags for channels 1 and 2 are set, the D-A conversion value output of the corresponding channels is set to "enabled". • If a D-A conversion value output needs to be set to "disable", reset the corresponding D-A conversion enable flag.	Y10 – D-A conversion value output enable flag for channel 1 Y11 – D-A conversion value output enable flag for channel 2
Y18	Error reset signal	• Turning ON the error reset signal resets the error flag, and clears the check code of the buffer memory. It is replaced by "0".	

3.7 Buffer Memory

The AI162DA has a buffer memory (not battery backed) for data communication with the CPU.

The buffer memory assignment and data maps are indicated below.

3.7.1 Buffer memory assignment

The following figure shows the buffer memory assignment

Address (Decimal)		Initial Value	Read	Write	Relevant Section
0	Analog output enable/disable channel	0	Enabled	Enabled	Section 3.7.2
1	CH.1 digital value	0	Enabled	Enabled	Section 3.7.3
2	CH.2 digital value				
3 to 8	Prohibited	—	—	—	—
9	Resolution of digital value	1(X1)	Enabled	Enabled	Section 3.7.4
10	CH.1 set value check code	0	Enabled	Enabled	Section 3.7.5
11	CH.2 set value check code				
12 to 17	Prohibited	—	—	—	—

Fig. 3.6 Buffer Memory Assignment

3.7.2 Analog output enable/disable channel area (Address 0)

(1) Defines the output enable/disable for the converted analog value per channel.

(2) All channels are enabled for output when:

(a) Power is switched on; or

(b) CPU is reset.

(3) Output disable/enable is defined by 1/0.

(a) 1.....Disable

(b) 0.....Enable

(4) The analog output enable/disable channel area data map is shown below:

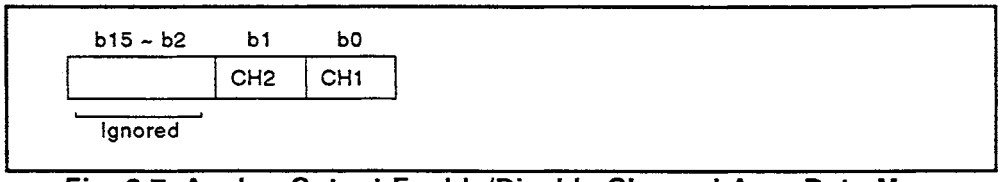


Fig. 3.7 Analog Output Enable/Disable Channel Area Data Map

3.7.3 CH.1 and CH.2 digital value area (Addresses 1 and 2)

(1) Write digital values to this area from the CPU for D-A conversion.

(2) Digital values of all channels are set to 0 if:

(a) D-A conversion ready (X1) is ON after power on; or

(b) D-A conversion ready (X1) is switched ON after the CPU is reset.

(3) Any digital value specified should be a 16-bit signed binary within the setting range of the digital value resolution. Any digital value outside this range is changed to a value indicated below before D-A conversion, and the corresponding check code is written to the set value check code area (addresses 10 and 11).

Table 3.6 The Setting Range of Digital Value

Output	Digital Value Resolution	Setting Range	Digital value for D-A conversion when values outside the special ranges are set.
Voltage output	1/4000	–4096 to 4095 (practical range: –400 to 4000)	4096 and above: 4095 –4097 and below: –4096
	1/8000	–8192 to 8191 (practical range: –8000 to 8000)	8192 and above: 8191 –8193 and below: –8192
	1/12000	–12288 to 12287 (practical range: –12000 to 12000)	12288 and above: 12287 –12289 and below:–12288
Current output	1/4000	0 to 4095 (practical range: 0 to 4000)	4096 and above: 4095 –1 and below:0
	1/8000	0 to 8191 (practical range: 0 to 8000)	8192 and above: 8191 –1 and below:0
	1/12000	0 to 12287 (practical range: 0 to 12000)	12288 and above: 12287 –1 and below:0

3.7.4 Resolution setting area of digital value (Address 9)

(1) The resolution set in the resolution setting area of digital value which corresponds to the range of analog output voltage is common to all channels.

(2) The resolution value of digital value is "1" (1/4000) in the following cases.

(a) At power on.

(b) At reset of the PLC CPU.

(3) The setting value should be 1, 2 or 3.

Table 3.7 Resolution Setting Range

Setting Value	Resolution of Digital Value
1	1/4000
2	1/8000
3	1/12000

POINT

(1) If the set value is other than 1, 2 or 3, the resolution value is not changed and is set to the last set value or to a default value.

(2) Change the resolution setting only one time before setting the D-A conversion output enable flag when a PLC CPU is in RUN.

When the setting of resolution value is changed during D-A conversion processing, a set value error will occur or an analog output will change.

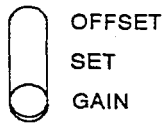
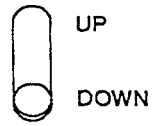
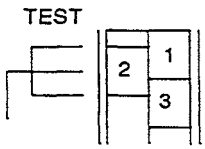
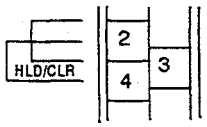
3.7.5 CH.1 to CH.2 set value check code storage area (Addresses 10 and 11)

(1) Used to check whether the set digital values are within or out of the setting range of digital value resolution.

(2) The corresponding check code in Table 3.8 is stored if a digital value out of the setting range of digital value resolution is set.

Table 3.8 Check Code List

Check Code	Description
000FH	A digital value over the setting range of digital value resolution was set.
00F0H	A digital value below the setting range of digital value resolution was set.
00FFH	Digital values over and below the setting range of digital value resolution were set. For example, the 00FFH check code is stored if a digital value exceeding the valid range is written, and then, without the check code being reset, a digital value that falls short of the valid range is written.

No.	Description	Application
(3)	OFFSET/GAIN select switch  	OFFSET position : Sets the offset value. GAIN position : Sets the gain value. SET position : The offset/gain value is stored to the A1S62DA internal memory when the switch is moved from "OFFSET"/"GAIN" to "SET".
(4)	UP/DOWN switch  	Increases or decreases the offset/gain value for the specified channel.
(5)	Test mode terminals  	Connected between terminals No.1 and No.3 to set the offset/gain values
(6)	Output HOLD/CLEAR setting terminals  	Used to hold or clear the analog output at the time of CPU STOP. Disconnected between terminal No. 2 and No.4 : CLEAR Connected between terminal No.2 and No.4 : HOLD

4.4 HOLD/CLEAR Setting of the Analog Output

This section explains how to define a HOLD/CLEAR setting of the analog output when the CPU is in the STOP mode.

(1) Use the HOLD/CLEAR terminal (on the front of the A1S62DA module) to define the HOLD/CLEAR setting of analog output.

Table 4.1 describes the settings and their status.

Table 4.1 HOLD/CLEAR Setting

Analog Output Setting	Status of the HLD/CLR Terminal (between terminal Nos. 2 and 4)
HOLD	Connected
CLEAR	Not connected

The original (factory-set) analog output status is CLEAR (disconnected).

(2) The analog output status of the HOLD/CLEAR setting varies with the settings of the D-A conversion value output enable flag (see Section 3.4.2) and the analog output enable/disable state (see Section 3.7.2).

Table 3.3 shows the analog output status for the settings of the D-A conversion value output enable flag and the analog output enable/disable state.

4.5 Offset/Gain Setting

(1) The offset and gain values are factory-set to the voltage outputs indicated in Table 4.2.

Table 4.2 Factory-set Offset/Gain Values

	Voltage Output
Gain value	10 V
Offset value (V)	0 V

(2) The offset and gain values may be changed and fine tuned in the test mode.

4.5.1 Notes on offset/gain setting

(1) Do not select the test mode during execution of the D-A conversion. By selecting the test mode D-A conversion of all channels stops, affecting control of the external devices. Returning from the test mode to the normal mode resumes D-A conversion with new offset/gain values.

(2) Offset/gain setting is allowed within the following ranges:

(a) Voltage.....–10 V to 0 V to +10 V

(b) Current..... 0mA to 20mA

If any value is set outside of the above range, overall accuracy may not be within the performance specifications range (see Section 3.2).

(3) The defined value is stored when the OFFSET/GAIN select switch is set to the "SET" position.

The offset and gain value remain unchanged if the test mode is terminated with the OFFSET/GAIN select switch in the "OFFSET" or "GAIN" position.

(4) Before switching from one channel to another in the test mode, the OFFSET/GAIN select switch should be in the "SET" position.

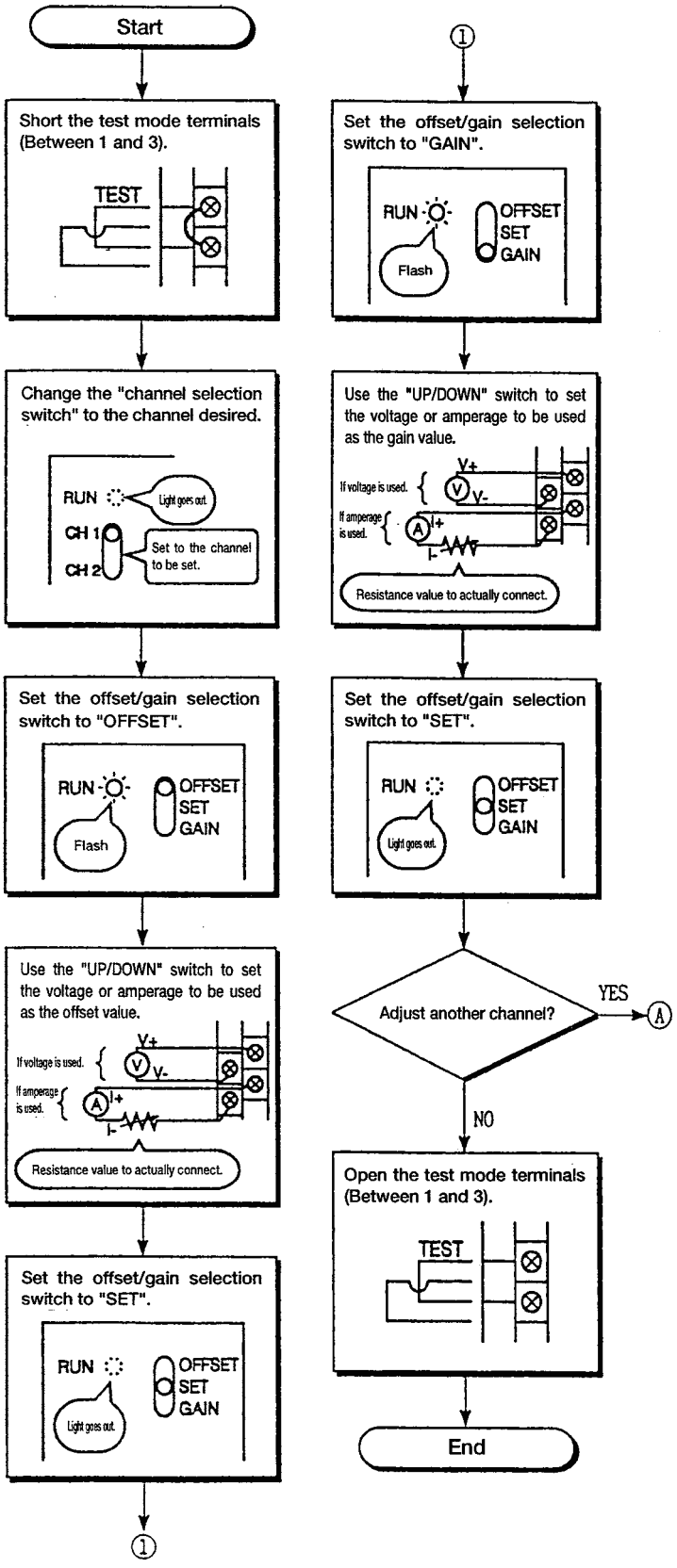
If the channel remains unchanged, the set value is stored to the new channel when the switch is set to "SET".

(5) The "RUN" LED light flashes quickly, at one-tenth (0.10) of a second intervals to indicate that the offset/gain specified has exceeded the allowed range.

When the "RUN" LED is flashing quickly, the offset/gain value remains unchanged if the OFFSET/GAIN select switch is in the "SET" position.

4.5.2 Offset/gain setting procedure

The following shows the offset/gain setting procedure.



4.6 Wiring

This section explains the wiring instructions and connection of the A1S62DA and the external devices.

4.6.1 Wiring instructions

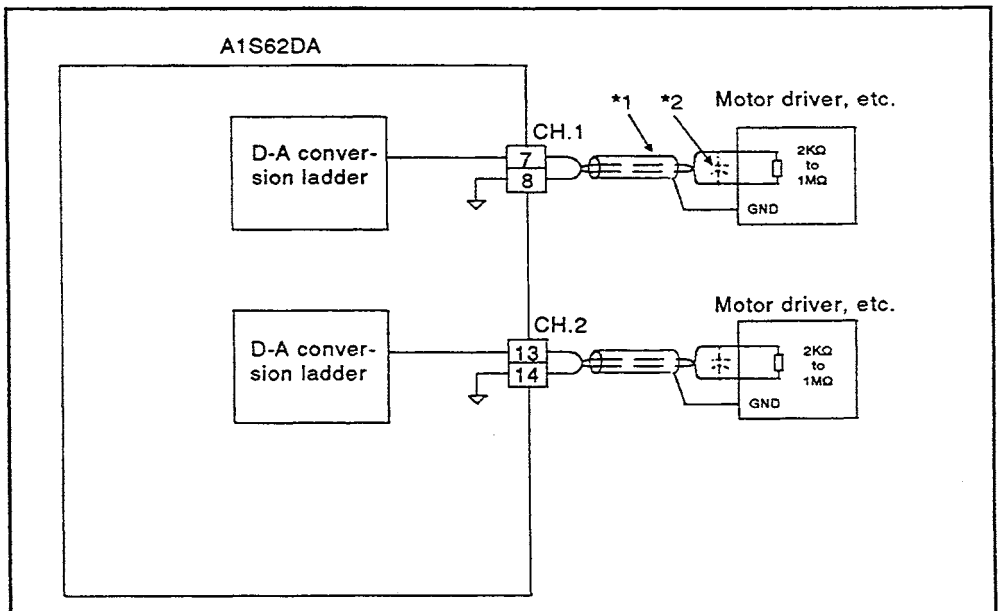
Protect the external wiring against noise with the following precautions:

(1) Separate the main circuit and/or high voltage wiring from the control and signal wiring.

(2) Where applicable, ground the shielding of all wires to a common ground point.

4.6.2 Connection of A1S62DA and external devices

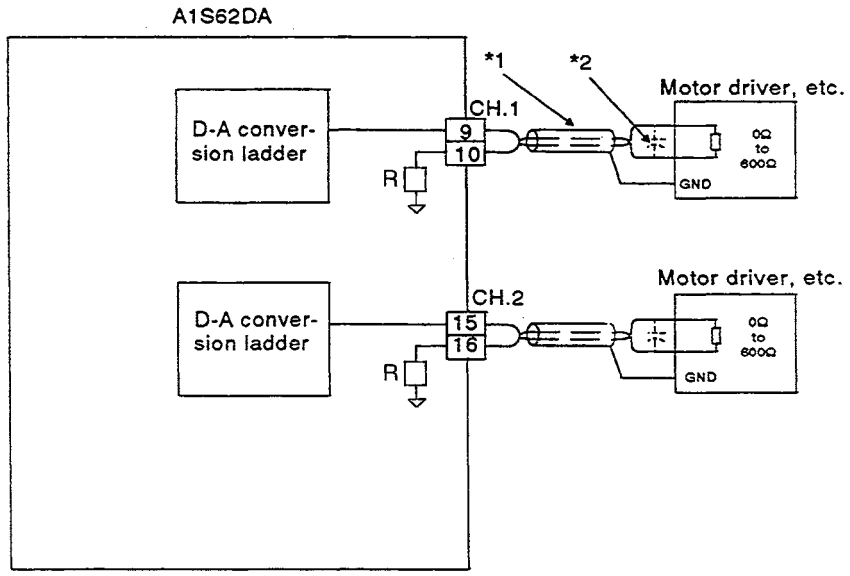
(1) The following figure shows the wiring example of the external devices in case of voltage output.



* 1: Use two-core shielded wiring (twisted).
* 2: If noise or ripple is generated by the external wiring, connect a 0.1 to 0.47 μF (25V or more voltage resistance parts) capacitor to the input terminal of the external device.

Fig. 4.3 Connection Example of the External Devices in case of Voltage Output

(2) The following figure shows the wiring example of the external devices in case of current output.



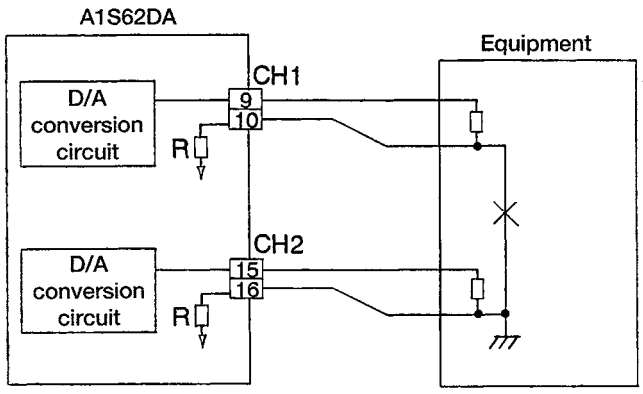
* 1: Use two-core shielded wiring (twisted).
* 2: If noise or ripple is generated by the external wiring, connect a 0.1 to 0.47 μF (25V or more voltage resistance parts) capacitor to the input terminal of the external device.

Fig. 4.4 Connection Example of the External Devices in case of Current Output

IMPORTANT

(1) The voltage and current output for the same channel cannot be used simultaneously.
Always open any terminals that are not being used as it is possible that if they are used they could cause damage to the internal elements.

(2) If current output is used, I-(COM) will become common and cannot be connected with equipment.
The output will normally cease.



5. PROGRAMMING

This section explains the programming procedure when using the A1S62DA.
When applying any of the program examples introduced in this chapter to the actual system, full verify that there are no problems in the controllability of the target system.

5.1 Programming Procedure

Program data transfer between the CPU and A1S62DA is indicated in Fig. 5.1.

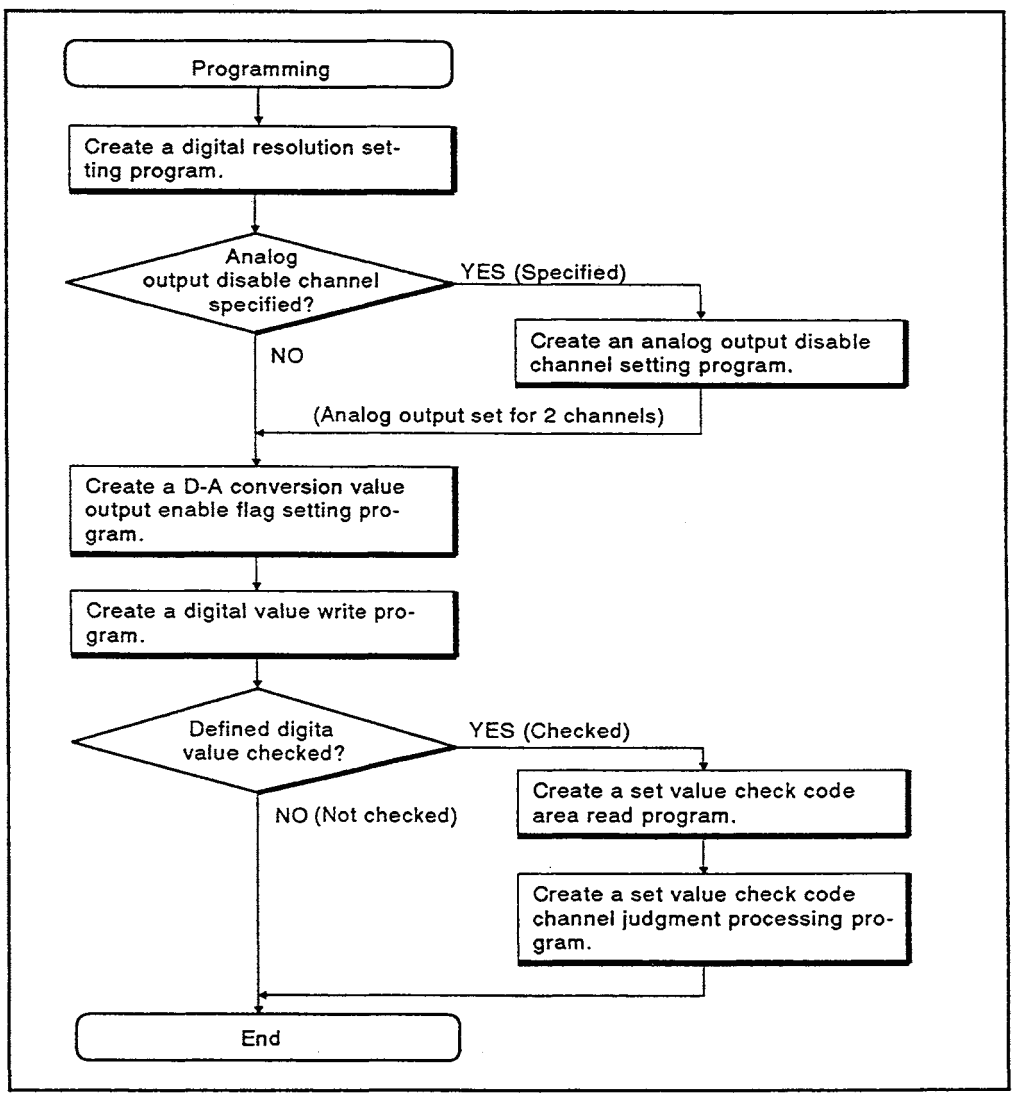


Fig. 5.1 Programming Procedure

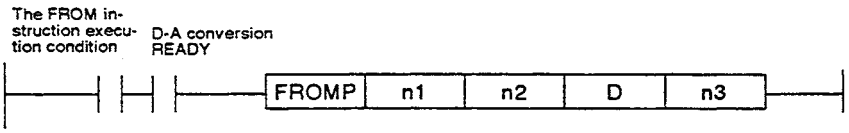
Point

During each of the processes of the special function module, access from the PLC CPU will have priority.
Accordingly, if frequent access to the buffer memory of the special function module made from the PLC CPU, it will not only extend the scan time of the PLC CPU, delays in each of the processes of the special function module will occur.
Only use the FROM/TO and other such commands to access the buffer memory from the PLC CPU when necessary.

5.2 Basic Program for Read/Write

(1) Read from A1S62DA ... FROM, FROMP, DFRO, and DFROP instruction

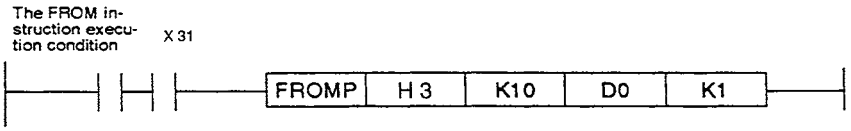
Format



Symbol	Description	Device That Can be Used
n1	The first two (2) digits when the head I/O number is allocated to A1S62DA in three (3) digits of hexadecimal	K, H
n2	Head address of the buffer memory in which data is stored	K, H
D	Head number of the device in which data is stored	T, C, D, W, R
n3	Number of words of read data	K, H

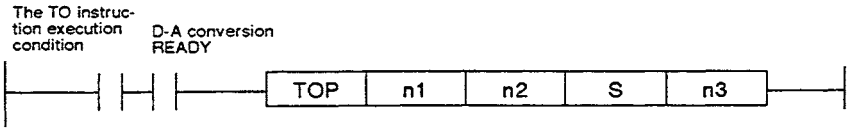
Example

When the A1S62DA is assigned to I/O X30 to 4F and Y30 to 4F, the data is read from address 10 of the buffer memory to one (1) word D0.



(2) Writing to A1S62DA ... TO, TOP , DTO, and DTOP instruction

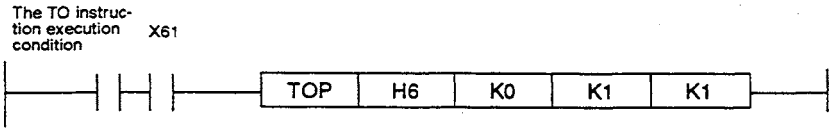
Format



Symbol	Description	Device That Can be Used
n1	The first two (2) digits when the head I/O number is allocated to A1S62DA in three (3) digits of hexadecimal	K, H
n2	Head address of the buffer memory in which data is stored	K, H
S	Number or constant of a head device in which writing data is stored	T, C, D, W, R, K, H
n3	Number of words of write data	K, H

Example

When A1S62DA is allocated to I/O X60 to 7F and Y60 to 7F, 1 is written in address 0 of a buffer memory



5.3 Program Example

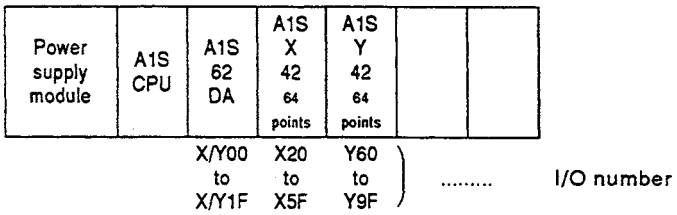
Write a value set by a BCD digital switch to the digital value setting area(address 1 of buffer memory) of channel 1 of A1S62DA.

If the written digital value has an error, a check code is read from the set value check code area (address 10 of a buffer memory) and is output to Y60 - Y62.

The following shows the program example.

Condition of a program example

(1) System configuration



(2) Initial setting

(a) Analog output enable channel ..... 1 channel

(b) Resolution ..... "1"(1/4000)

(3) Device to be used by user

(a) Initial setting input command signal X20

(b) Digital value input command signal X21

(c) Setting of a digital value (4 digits in BCD) ..... X30 to X3F

(d) Error indication command signal X22

(e) Error reset command signal X23

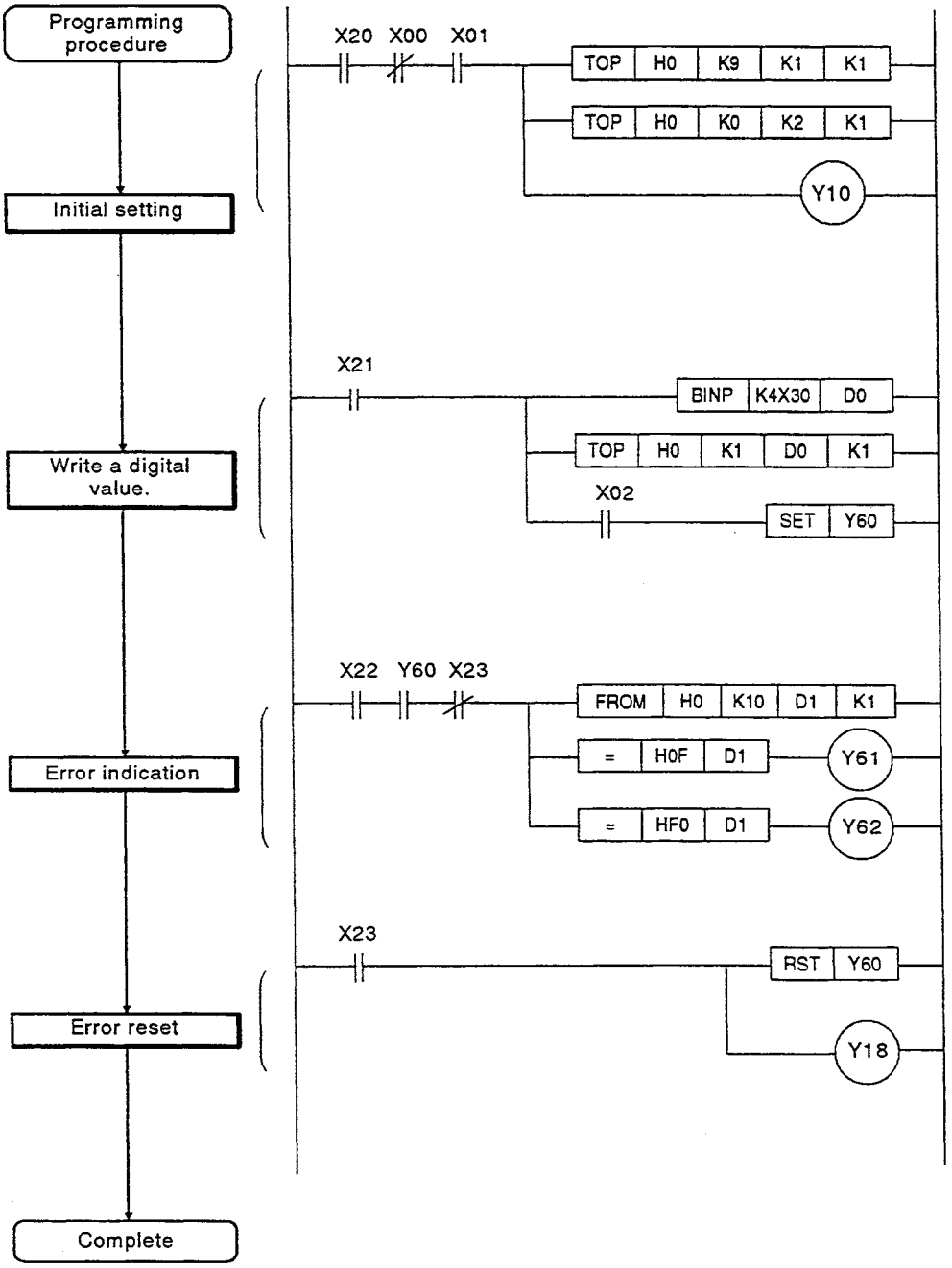
(f) Digital value storage register D0

(g) Check code storage register D1

(h) Digital value setting error output Y60

(i) A digital value of 4096 or more is set. Y61

(j) A digital value of -4097 or less is set. Y62



Set the resolution of a digital value to 1/4000.

Set channel 1 to analog output permission, and set channel 2 to an analog output disable channel.

When the WDT error flag is reset, and a D-A converter READY flag is ready, set the output enable flag of channel 1.

Convert an input (X30 to X3F) into binary from the BCD digital switch, and store it in D0.

Write the value of D0 in address 1 of a buffer memory.

When an error flag is ready, set Y60.

When an error occurs, read a check code from address 10 of the buffer memory to D1.

If the set value is 4096 or more, set Y61.

If the set value is -4097 or less, set Y62.

Reset an error indication and a check code.

6. TROUBLESHOOTING

Assorted problem conditions and a troubleshooting guide for the A1S62DA are described below. For information on the CPU module, see the corresponding CPU User's Manual.

6.1 When the RUN LED Flashes or Goes OFF

(1) When the RUN LED goes OFF:

Items to Check	Corrective Actions
Are the TEST terminals shorted? (Test mode)	Make offset/gain adjustments, and then open the TEST terminals.
Has an error occurred in the CPU module?	Refer to the appropriate User's Manual for error information, and correct the error.
Is the power supply module (5 VDC) that is installed to the base unit not getting enough current?	Recalculate the total number of amps for the CPU, I/O module, and special function module installed to the base unit, and replace the power supply module if necessary.
Is the A1S62DA WDT error flag set?	Reset the CPU module.

(2) When the RUN LED flashes:

Items to Check	Corrective Actions
Are the TEST terminals shorted when offset/gain select switch is set to OFFSET or GAIN? (Test mode)	Set the offset/gain, and then open the TEST terminals.
Does the LED flash at one-tenth (0.10) of a second intervals when in the test mode?	Reset the CPU module.
Is the digital value outside the setting range written?	Clear the setting value check code storage area with an error reset flag.

6.2 When the Analog Value is 0 V/0 mA

(1) When the values of all channels are 0 V/0 mA:

Items to Check	Corrective Actions
Is the RUN LED of the A1S62DA turned OFF?	Follow procedures in Section 6.1.
Are the analog output enable/disable channels of each channel set to disable?	Set the analog output enable/disable of the channels to be used to enable.
Is the WDT error flag set?	Follow procedures in Section 6.7.
Is the D-A conversion ready flag set?	Follow procedures in Section 6.8.
Is the digital value written in the digital value setting area (addresses 1 and 2) of the buffer memory?	Write the digital values of the channel to be converted from digital to analog. (See Sections 3.7.3 and 5.2.1.)

(2) When the value of a given channel is 0 V/0 mA:

Items to Check	Corrective Actions
Is the analog output enable/disable channel with its "0 V/0 mA" analog value set to disable?	Confirm the data set in the analog output enable/disable channel setting area of the buffer memory. (See Section 3.7.2.)
Is the digital value of the channel with its "0 V/0 mA" analog value written in the digital value setting area of the buffer memory?	Write the digital value. (See Section 3.7.3.)
Is the external wiring done correctly?	Make sure the external wiring is correct.

6.3 When Analog Values are Offset Values

(1) When the analog values of all channels are offset values:

Items to Check	Corrective Actions
Are the TEST terminals shorted? (Test mode)	Make offset/gain adjustments, and then open the TEST terminals.
Is the RUN key switch of the CPU module set to a position other than "RUN"?	Set the switch to the RUN position.
Are the D-A conversion value output enable flags of each channel reset?	Set the D-A conversion value output flags of the channels to be used.
Is the digital value written in the digital value setting area (addresses 1 and 2) of the buffer memory?	Write the digital values of the channel to be converted from digital to analog. (See Sections 3.7.3 and 5.3.)

(2) When the analog value of a given channel is an offset value:

Items to Check	Corrective Actions
Is the D-A conversion value output enable flag setting for a channel whose analog value is an offset value reset?	Set the D-A conversion value output enable flag.
Is the digital value of the channel whose analog value is an offset value written to the digital value setting area of the buffer memory?	Write the digital value. (See Section 3.7.3.)

6.4 Analog Values are Output Although the CPU Module is Set to STOP

(1) When the analog output does not change after setting to STOP.

Items to Check	Corrective Actions
Are the HOLD/CLEAR setting terminals shorted (held)? • Is the D-A conversion value output enable flag of the channel outputting analog values set to enable? • Is the enable/disable output of the channel outputting analog values set to enable?	If one or more of these conditions exist, make the necessary corrections. (See Section 3.4.)

(2) When the analog output changes after setting to STOP:

Items to Check	Corrective Actions
Is the outputted analog value offset value?	Confirm the offset value. When making the output value 0 V/0 mA, set the offset again.

6.5 When Analog Values Output although the Output Enable Flag (Y10 and Y11) is Reset

(1) When offset values are output:

Items to Check	Corrective Actions
Are the HOLD/CLEAR setting terminals shorted (held)? • Is the D-A conversion value output enable flag of the channel outputting offset values set to disable? • Are the HOLD/CLEAR setting terminals shorted (HOLD)? • Is the analog output enable/disable channel for outputting analog values set to enable? • Is the digital value not set to "0"?	If one or more of these conditions exist, make the necessary corrections. (See Section 3.4.)

(2) When analog values (except offset values) are output:

Items to Check	Corrective Actions
Are the HOLD/CLEAR setting terminals shorted(held)? • Are the HOLD/CLEAR setting terminals of analog output shorted (HOLD)? • Is the D-A conversion value output enable flag of the channel outputting analog values set to enable? • Is the analog output enable/disable channel for outputting analog values set to enable? • Is the digital value not set to "0"?	If one or more of these conditions exist, make the necessary corrections. (See Section 3.4.)

6.6 When Digital and Analog Values do not Match

(1) When both digital values and analog values change:

Items to Check	Corrective Actions
Does the digital value match the analog value?	Correct the offset/gain values.
Are the A1S62DA and external devices properly wired?	Make sure the wiring between the A1S62DA and the external devices is correct.
Is the digital values written in the digital setting area (addresses 1 and 2) incorrect?	Write the proper values to the addresses of the corresponding channels in the buffer memory.

(2) When the digital value changes and the analog value is fixed:

Items to Check	Corrective Actions
Is the RUN key switch of the CPU module set to a position other than "RUN"?	Set the switch to the RUN position
Is the digital value written in the digital value setting area of the buffer memory (addresses 1 and 2)?	Write the digital value of the channel to be converted from digital to analog. (See Sections 3.7.3 and 5.3.)

6.7 D-A Conversion READY Flag (X1) is Reset

Items to Check	Corrective Actions
Is there an error in the CPU module?	See the corresponding User's Manual for the respective CPU module for error information. Correct the error.
Is there an I/O number error?	Confirm and correct the I/O number.
Are the TEST terminals shorted? (Test mode)	Open the TEST terminals and cancel the test mode.

6.8 Error Flag (X2) is Set

Items to Check	Corrective Actions
Is a value that is not "0" set in the setting value check code storage area (addresses 10 and 11) of the buffer memory?	Verify that a digital value outside the setting range was written in which data other that "0" is stored to a channel and its corresponding check code storage area. Clear the set value storage area with the error reset flag (Y18).

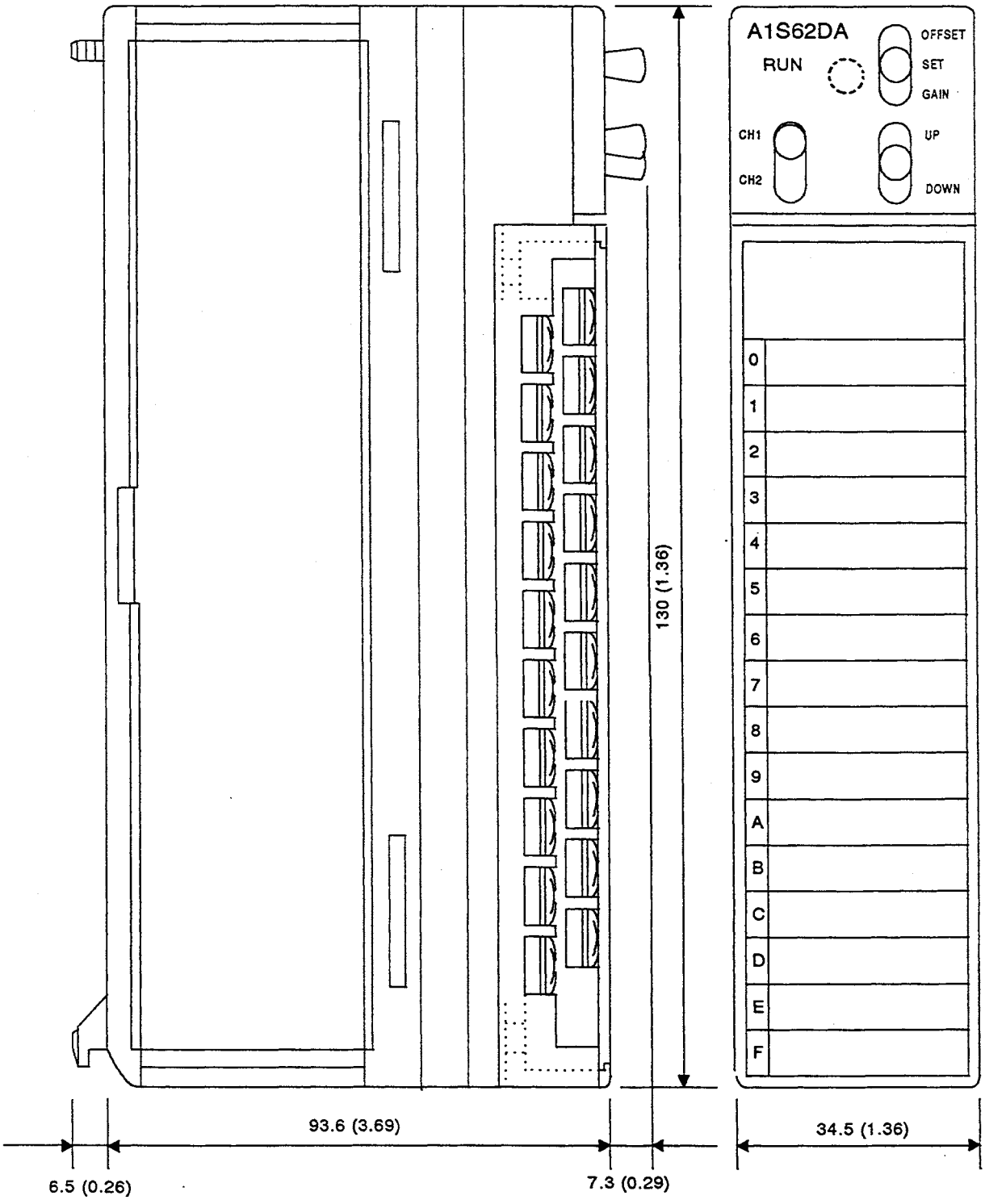
POINT

If these corrective measures do not solve the problem, there may be a hardware malfunction in the module.

Consult a Mitsubishi representative.

APPENDICES

Appendix 1 Outside Dimensions



Unit: mm (in)

Appendix 2 Signal Paper

Front

0	
1	
2	
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9	
A	
B	
C	
D	
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F	

Back

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MEMO

MEMO

WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.
However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.
Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.
(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.
1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.
(2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation of damages caused by any cause found not to be the responsibility of Mitsubishi, loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products, special damages and secondary damages whether foreseeable or not , compensation for accidents, and compensation for damages to products other than Mitsubishi products, replacement by the user, maintenance of on-site equipment, start-up test run and other tasks.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to change without prior notice.

6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.
(2) The Mitsubishi programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for Railway companies or Public service purposes shall be excluded from the programmable logic controller applications.
In addition, applications in which human life or property that could be greatly affected, such as in aircraft, medical applications, incineration and fuel devices, manned transportation, equipment for recreation and amusement, and safety devices, shall also be excluded from the programmable logic controller range of applications.
However, in certain cases, some applications may be possible, providing the user consults their local Mitsubishi representative outlining the special requirements of the project, and providing that all parties concerned agree to the special circumstances, solely at the users discretion.

D/A Converter Module Type A1S62DA

User's Manual

MODEL	A1S62DA-U-E
MODEL CODE	13J673
IB(NA)-66335-E(0609)MEE	

MITSUBISHI ELECTRIC CORPORATION

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When exported from Japan, this manual does not require application to the Ministry of Economy, Trade and Industry for service transaction permission.

Specifications subject to change without notice.